

SECTION 34 42 19

MICROPROCESSOR – BASED INTERLOCKING HARDWARE

PART 1 - GENERAL

1.01 SECTION INCLUDES

- A. Vital Microprocessor Based Interlocking Controller

1.02 RELATED SECTIONS

- A. Interface and coordinate the work of this Section with Section 20 70 23 – Electronic Circuits Wires and Cables, Section 34 42 24 – Train Control Room Equipment

1.03 MEASUREMENT AND PAYMENT

- A. General: Microprocessor-based interlocking hardware, as specified herein, will not be measured separately for payment but will be paid for as part of the Contract lump sum price for Automatic Train Control System Work as indicated in the Bid Schedule of the Bid Form.

1.04 REFERENCES

- A. American Society for Testing and Materials (ASTM):
 - 1. ASTM A167 Stainless Steel
 - 2. ASTM B36 Cartridge Brass
 - 3. ASTM B140 Commercial Bronze
- B. Federal Standards (FS):
 - 1. FS QQ-S-766 Steel, Corrosion Resistant
 - 2. FS QQ-N-290 Nickel Plating, Electrodeposited
- C. Institute for Printed Circuits (IPC):
 - 1. IPC-CM-770E Guidelines for Printed Board Component Mounting
- D. Military Standards:
 - 1. MIL-G-45204 Gold Plating; Electrodeposited
 - 2. MIL-C-50 Copper Alloy Number 260 (Cartridge Brass)
 - 3. MIL-STD-10 Surface Roughness, Waviness, and Lay
 - 4. MIL-STD-105 Sampling Procedures and Tables for Inspection by Attributes

5. MIL-STD-202 Test Methods for Electronic & Electrical Component Parts

1.05 SUBMITTALS

- A. General: Refer to Section 01 33 00 - Submittal Procedures, and Section 01 33 23 - Shop Drawings, Product Data, and Samples, for submittal requirements and procedures.
- B. Submit the following drawings, data, and procedures for approval prior to furnishing and installing the equipment:
1. Complete system data flow and software architecture diagrams for all VMIS modules of the system and all interfaces to the system.
 2. Complete circuit drawings and systems diagrams, in a manner as hereinafter specified, for all system and subsystem interfaces, including interconnections of all hardware to the system.
 3. Complete power distribution circuit drawings and schematics, as hereinafter specified.
 4. Complete rack layout and arrangement plans.
 5. Complete equipment plans and installation drawings showing all components of the system. These drawings shall include complete keyed parts lists for all components of the system, racks, terminal boards, plug connectors, cable boots, mounting hardware, and all other rack mounted equipment and hardware.
 6. Software listings and logic diagrams for application dependent software.
 7. Drawings showing details of interconnecting cables, plug couplers, terminal boards, and other interconnecting devices complete with keyed parts lists and cable assembly instructions.
 8. Complete predicted Reliability and Maintainability (R&M) calculations. Actual performance data for a like system for which reliability records have been maintained for a period of not less than three (3) years, may be used to support or substantiate the submitted predicted R&M calculations
 9. Complete power calculations for all power sources energizing the vital controllers or controlled, or switched, by vital controllers. Where manufacturer's specific ripple or regulation specifications exist for the vital controllers or associated equipment relying upon these power sources, compliance with such ripple or regulation specifications shall be demonstrated to the satisfaction of the Engineer.
 10. Factory Test Procedures designed to demonstrate that the manufactured system will be tested to verify that it performs all functions in accordance with these specifications and in accordance with the approved plans.
 11. Subsequent to Factory Testing, certified factory test reports.
 12. Complete and comprehensive Installation and Inspection Procedures.

13. Field Test Procedures in accordance with the testing section of these Specifications to verify that the installed system meets all safety and operational requirements of these Specifications and that it has been installed in accordance with the final approved plans.
 14. Field Test Reports complete with data results.
- C. The Contractor shall provide ten (10) complete sets of application, service, and development system manuals, including manuals covering all software and hardware provided as part of the application software development system required as part of this Contract.

1.06 QUALITY ASSURANCE

- A. The system shall be designed to operate in accordance with all applicable AREMA recommendations for the control and indication of interlocking safety functions.
- B. The design of the system shall comply in every respect with the latest Rules and Regulations Governing Railroad Signal and Train Control Systems as issued by the office of Safety, Federal Railroad Administration, and of any supplements thereto that become effective before this Contract is awarded.
- C. The Contractor shall certify that the entire vital microprocessor system type being furnished under this Contract has been tested to successfully operate in the high electric background noise environment of an operating railroad. The system shall comply with the requirements of MIL STD 461 where applicable to a railroad type environment.
- D. The Contractor shall certify that the proposed type system has been successfully operated after being exposed to vibration of 2-10 Hz, 0.2-inch displacement, peak-to-peak and 10-500 Hz at 1.0 G as prescribed by MIL STD 810C, method 514.2, category F, and to shock of 3 G as prescribed by MIL STD.810C method 516.2, Sawtooth Procedure I, Transit Drop Procedure I.
- E. All components of the system, except LCD terminals and printers shall be capable of continuous operation at temperatures of -40 degrees F to 160 degrees F and humidity levels of 5% to 95%, noncondensing, without the need of any external environment controls. The LCD terminals and printers shall be capable of continuous operation at temperatures of 0 degrees F to 105 degrees F and humidity levels of 10% to 95%.
- F. No failure of any component of the vital controllers shall cause the vital microprocessor interlocking system to falsely or erroneously maintain for any reason a permissive state.
- G. Printed circuit board pin and socket contacts shall be in accordance with the specified Standards.

1.07 SHIPMENT AND HANDLING

- A. Equipment furnished under this Section shall not be shipped until the Engineer has approved the factory test reports, in writing.
- B. Each item of the VMIS shall be inspected by the Contractor and the Engineer for shipping damage prior to installation.
- C. Any equipment showing signs of damage shall be repaired or replaced, at the Engineer's

option, without any additional cost to the Contract.

- D. Equipment shall be shipped in suitable crating and shall be properly braced to prevent damage during shipment.

PART 2 – PRODUCTS

1.00 GENERAL REQUIREMENTS

- A. The Work includes furnishing, testing, and documenting pre-wired vital microprocessor based interlocking controller racks and local control panels that provides the functionality as shown on the Contract Drawings. BART will furnish vital application logic programs in ladder logic or Boolean equation format.
- B. The interlocking controller and all components associated therewith must have a demonstrable history of safe and reliable use in revenue operation in a similar operating environment to that of the existing BART commuter rail/rapid transit operation.
- C. Protection against surges, spikes and over-voltage shall be provided. The Contractor shall protect all power feeds, input and output leads, and all other auxiliary equipment with lightning and surge protection as necessary.
- D. Interconnection with non-vital supervisory control equipment shall be as shown on the Contract Drawings and as specified herein. Interface with other vital field signal control systems shall be as required to provide failsafe control of the signal system.
- E. The interlocking controller or Vital Microprocessor Interlocking System (VMIS) as herein specified shall be designed on the basis of closed loop principles, software diversity and use of proven vital hardware design techniques to achieve safety. The use of multiple processor arrangements based upon voting to enhance the probability of achieving safety is not acceptable.

2.02 DESIGN REQUIREMENTS

- A. BART presently uses GETS VHLC'S and Alstom VPI's for their Vital Micro processor systems. If the Contractor chooses to use another type system, in accordance with these specifications, the Contractor shall provide a complete spare unit for maintenance purposes. Additionally the Contractor shall provide training in the programming, set up and testing of the alternate system. The training will be for a 4-week period for BART's Engineering and Maintenance personnel. BART will provide the application dependent software for a VHLC or VPI system. If the Contractor uses a different system then it shall be the Contractors responsibility to convert the application software to work with the approved system. The VMIS design shall be based upon solid state microprocessor technology and shall not require any off-line storage devices for operation or start up. The operation of the system shall be programmed in solid-state memory. In addition, other functions as specified herein shall be part of this system.
- B. Instrument Rack Arrangement Plans shall be as shown in the Contract Drawings. The placement of all rack-mounted components shall be clearly shown. Front, side, and rear views shall be shown on each rack arrangement plan. Only one instrument rack shall appear on each

sheet. All rack grounding and component grounding details shall be shown.

- C. All plug-connected cables associated with the instrument rack shall be identified by reference numbers and shall be shown connected to the proper plug receptacle.
- D. Cable Assembly Drawings shall be furnished for all cables employed by the interlocking system. All plug or receptacle pin assignments shall be shown. All wire gauge, wire color-coding, and wire lengths shall be shown. Shield grounding arrangements shall be shown. A list of tools required and instructions for fabrication of the cables shall be provided on the drawings. All parts or materials necessary for reordering shall be shown and identified with a reference number. This reference number shall correspond with a tabulation of material showing part numbers and quantities included on the cable assembly drawings.
- E. Complete Cable Schematic Drawings shall be furnished for all data communications cables employed by the system. All plug or receptacle assignments shall be shown. All wire color-coding, functional wire nomenclature, and plug, slot, and rack or card file destinations shall be shown.
- F. Complete Circuit Drawings shall be designed and furnished. All hardwire input and output circuit drawings shall be shown complete with all terminal designations, terminal board locations, printed circuit board edge connector or plug connector designations, and functional wire nomenclature. Card file or rack number and slot locations of all printed circuit boards shall be shown.
- G. Signal Lighting Circuit Drawings shall include all wires and termination points from the printed circuit cards to the signal lamps on one sheet.
- H. Switch Operating Circuit Drawings shall include all wires and terminations from the printed circuit boards to the switch control relays on one sheet.
- I. Switch Indication Circuit Drawings shall show all wires and terminations from the printed circuit boards to the entrance racks.
- J. Track Repeater Circuit Drawings shall show all wires and terminations from the printed circuit boards to the track relays.
- K. Wire sizes shall be clearly identified on each circuit drawing.
- L. Power distribution schematics shall be furnished showing all rectifiers, power supplies, terminals, cables, busses, wires, and wire sizes for all power sources energizing the vital controllers or controlled or switched by the vital controllers. LED equipped rail mounted terminal blocks shall be utilized for all power to the VMIS, the VMIS I/O, and the VMIS serial controllers.
- M. The VMIS application software documentation shall be provided, showing progression of switch control from the supervisory system inputs to the switch control relays, examples of route, time, and switch locking, progression of signal control from the supervisory system inputs to the signal lamps, and examples of all other logic executed by the vital interlocking system.
- N. All data passed from one vital controller to another vital controller and all data passed from

any vital controller to the supervisory system shall be identified as well as all hardware interfaces. All terms in the logic expressions and all data received by or sent from the controllers shall be identified with standard BART relay logic nomenclature. Translation tables will not be acceptable.

- O. The operating instructions for the VMIS shall be divided into application and executive dependent portions. The executive instructions shall be stored in solid state read only memory (ROM) or solid-state Programmable Read Only Memory (PROM) devices and shall be referred to as the Executive Firmware. The application dependent instructions shall be stored in solid-state Erasable Programmable Read Only Memory (EPROM) devices and shall be referred to as the Application Dependent Firmware. The executive firmware and application firmware shall reside in separate memory devices.
- P. A complete Application Dependent Firmware Development System shall be furnished as specified herein.
- Q. The Vital Processor Units shall be equipped with on-board diagnostics. These diagnostics shall quickly and reliably identify failed printed circuit boards. The nature of the failure as well as the specific location of the failure shall be indicated. All on board diagnostics shall be accessible to a dial-in telecom line for access by a/the remote diagnostics terminal.

2.03 VITAL CONTROLLER EXECUTIVE FIRMWARE

- A. The executive firmware shall continuously test for a loss of control over the state of the hardware outputs, a loss of control over RAM, a loss of vital data communications, and a spontaneous change in the application dependent firmware.
- B. The executive firmware shall log all vital and non-vital failures and identify the faulty printed circuit card or function.
- C. The executive firmware shall supervise a closed loop monitoring system for all hardware input and output functions.
- D. All functions required for system integrity evaluation, error logging, hardware interface, timing, data communications, application logic execution, and the application of power to the vital controller shall be fully interleaved and executed by the vital processor. Failure to pass any of the system integrity tests shall cause the system to cease all data communications and remove power, in a completely fail safe manner, from the hardware outputs.

2.04 APPLICATION DEPENDENT FIRMWARE

- A. The application dependent firmware shall define the operation of the VMIS; the operation of the individual functions shall be as indicated on the Contract Drawings and shall include, but not be limited to:
 - 1. Route Check
 - 2. Signal Control
 - 3. Signal Lighting

4. Signal Indication
 5. Time Locking
 6. Route Locking
 7. Switch Locking
 8. Switch Control
 9. Switch Indication
 10. Switch Correspondence
 11. Loss of Shunt
 12. Non-vital processing for the following controls:
 - a. Route setting including:
 - (1) Switch Operation
 - (2) Signal Operation
 - b. Route Cancellation
 - c. Auxiliary Functions
 13. Non-vital processing for the following indications:
 - a. Signal Operation
 - b. Switch Position
 - c. Switch Locking
 - d. Track Occupancy
 - e. Alarm and Auxiliary Status
 - f. System Failure Indication
 14. All necessary data communication conditioning including the building of repeaters.
- B. The application dependent firmware shall be keyed to the vital controller hardware rendering it impossible for any application dependent firmware to be executed in any vital controller other than the intended vital controller.
- C. The application dependent firmware shall be stored on an EPROM device and shall be replaceable without disturbing the executive firmware.

2.05 GENERAL HARDWARE AND OPERATING REQUIREMENTS

- A. The VMIS shall consist of a number of Vital Processor Units and the associated cables, plugs, wire connectors, terminal blocks, power conditioning equipment and hardware.
- B. Each Vital Processor Unit shall consist of printed circuit boards of the various types, as specified herein, mounted within card files in one instrument rack. VMIS units when mounted shall have access from the rear.
- C. All plug connectors, data transmission equipment, power supplies, power conditioning devices, terminal boards, wire connectors, and other equipment required to achieve a complete, stand-alone subsystem shall be mounted within the instrument rack along with the associated vital processor units.
- D. The vital processor units shall be provided with Double Break Vital Output Printed Circuit Boards (DBVO) and Vital Input printed Circuit Boards (VI) as specified herein. A sufficient number of these types of printed circuit boards shall be installed in each vital processor unit to accommodate all vital hardwire inputs and outputs.
- E. The vital processor units shall be provided with Non-vital Input/Output Printed Circuit Boards (NVI/NVO) as specified herein. A sufficient number of these type printed circuit boards shall be installed in the vital processors to accommodate all non-vital hardwire inputs and outputs.
- F. The hardware interface I/O board shall indicate, with logically grouped lights mounted on the interface boards, the status (Hi or Lo) of each input or output. An approved lamp labeling system shall be provided as part of the unit, visible when viewing the status lamps.
- G. The Vital Processor Units shall be provided with Vital Lamp Driver Printed Circuit Boards as specified herein. A sufficient number of these types of printed circuit boards shall be installed in each Vital Processor Unit to accommodate all vital signal lamp outputs within that Vital Processor Unit's scope of control.
- H. The use of external relays as interface devices between the Vital Processor Units and external circuits shall be as specified herein, or as indicated on the Contract Drawings. If the vital microprocessor interlocking units furnished by the Contractor require more external relays as interface devices than is shown on the contract drawings or specified herein, then it shall be the Contractor's responsibility to furnish such relays as part of the contract to provide a complete VMIS.
- I. The Vital Processor Units shall have a twenty percent (20%) expansion for storage of application dependent firmware and capability, through space, for additional printed circuit boards.
- J. Each Vital Processor Unit shall be provided with Vital Serial Communication Ports as specified herein. The number of Vital Serial Communication Ports shall be sufficient to allow interconnection of the Vital Processor Units in accordance with the Contract Drawings and as required. Communication of data between the Vital Processor Units shall be transmitted through these Vital Serial Ports.
- K. Each Vital Processor Unit shall also be provided with Non-Vital Serial Communication Ports as specified herein. The number of Non-Vital Serial Communication Ports shall be sufficient

to allow interconnection of the Vital Processor Units and the supervisory control system for data communication as indicated on the Contract Drawings. Non-vital serial communications ports shall be configured for communications via the fiber optic modems as specified herein.

- L. Each Vital Processor Unit card file(s) or pair of card files shall contain printed circuit boards of the types described herein. Additional types of printed circuit boards required for the operation of the Vital Processor Units shall be furnished and installed as required. Combination of functions among the board types shall be allowed only as specified herein.
- M. The printed circuit boards shall be housed within a card file and be of the plug-in type. Keys shall be provided on the card file to prevent the insertion of improper printed circuit board types.
- N. The card files shall be factory mounted in a standard 19 inch instrument racks. The rail mounted terminal blocks shall interface all wire connections to the cardfiles. No forced air ventilation shall be used.
- O. The design shall provide that all cables or wiring leaving the rack shall be routed through rubber boots at the top of the racks and be provided with means to be neatly routed and securely fastened with tie straps.
- P. All power conditioning including, but not limited to, surge and noise suppression required on the power feeds for the rack mounted power supplies shall be located on the VMIS rack.
- Q. The hardwire inputs of the vital controllers shall not respond to ac voltage levels. The hardwire inputs shall be biased and shall not, under any failure condition, respond to any voltage of improper polarity.
- R. The hardwire outputs of the vital controllers shall provide security equal to, or greater than, conventional double-break relay circuits for any circuits leaving the housing.

2.06 VITAL PROCESSOR UNIT PRINTED CIRCUIT BOARDS

- A. Each Vital Processor Unit shall be equipped with one Central Processing Unit Printed Circuit Board (CPU PCB). CPU PCBs throughout the Vital Processor System shall be identical with the exception of the instructions stored in the Application Dependent Firmware PROM and a keying system that shall prevent operation of the Vital Processor Units when a CPU PCB from another Vital Processor Unit is installed. This Contractor shall demonstrate that the keying system is designed according to accepted fail-safe principles. The CPU PCBs shall conform to the requirements shown below:
 1. The CPU PCBs shall contain the microprocessor, clock, random access memory (RAM), Executive Firmware, Application Dependent Firmware, data bus, address bus, and all other components of the computing portion of the system. Other printed circuit boards comprising the system shall be input-output adapters and interfaces only.
 2. The CPU PCBs may contain the hardware for the Vital and Non-vital Data Serial Communication Printed Circuit Boards as specified herein.
 3. The CPU printed circuit boards shall not perform any of the functions or affect any of the connections to external devices specified for the hardwire interface printed circuit boards.

4. The Application Dependent Firmware PROMS shall be mounted on the CPU printed circuit boards via sockets, the contacts of which shall be fabricated from commercial bronze or brass and plated with gold over nickel underplate.
 5. Wire jumpers and piggy back boards shall not be used unless permitted by the Engineer.
- B. Each Vital Processor Unit shall be equipped with one Non-Vital Serial Interface Printed Circuit Board (NVTI PCB). NVTI PCBs throughout the Vital Processor System shall be identical. The NVTI PCBs shall conform to the following requirements:
1. The NVTI PCBs shall contain two RS232C compatible serial ports.
 2. One port shall be configured as a master with the ability to initiate communications with and discretely address an approved number of other serial ports electrically connected to a common serial line. The maximum number of such slave ports shall be the manufacturer's standard.
 3. The slave port shall be configured with the ability to select one of an assigned number of address codes. The slave port shall receive and transmit data only when the master port connected to the common serial line specifies an address that corresponds to the slave port's address.
 4. Data transmission rates for all non-vital serial ports shall be independently adjustable. The method of adjustment, maximum adjustable bits per second (BPS), and optimum adjusted BPS shall be as approved by the Engineer.
 5. Communications protocol for all serial data communications lines shall be compatible with all connected devices, as indicated on the Contract Drawings, including fiber optic modems.
 6. Data communications cables shall be plug connected to the NVTI PCBs. Cable shielding shall be connected to ground on one end only.
- C. Each Vital Processor Unit shall be equipped with Vital Input Printed Circuit Boards (VI PCBs) as specified herein.
1. VI PCBs shall be furnished and installed in sufficient number to accommodate all vital inputs within the VMIS's scope of control including, but not limited to:
 - a. One input from each vital track relay front/heel contact.
 - b. One input from each switch and lock movement normal position indication circuit.
 - c. One input from each switch and lock movement reverse position indication circuit.
 - d. One input from each electrical switch lock normal position indication circuit.
 - e. One input for each possible polarity of each vital line circuit.
 2. The VI PCBs shall accept inputs without the use of external or board mounted interface

relays. Energy for the inputs shall flow directly from the relay contacts, line circuits, or signal equipment as described herein, through the specified cables and internal signal instrument house wiring.

- D. Each VMIS unit shall be equipped with Vital Output Printed Circuit Boards (VO PCBs) as specified herein.
 - 1. VO PCBs shall be furnished and installed in sufficient number to accommodate all vital outputs within the Vital Processor Unit's scope of control including, but not limited to:
 - a. Two outputs to each switch and lock movement controller relays.
 - b. One output for each possible polarity of each vital line circuit feed.
 - 2. The VO PCBs shall output energy directly to the relay coils, line circuits, or signal equipment as described herein, through the specified cables and internal signal instrument house wiring.

- E. Each Vital Processor unit shall be equipped with solid-state vital timers as specified herein.
 - 1. Vital timers shall be furnished in sufficient number to accommodate all vital timing functions within the Vital Processor Unit's scope of control, including, but not limited to:
 - a. Loss of shunt time for track repeater relays.
 - b. NPS timers for each signal.
 - 2. Vital timers shall be field settable and shall be selectable by a means other than by modification to the application software designed for the interlocking.
 - 3. Vital timer selection switches shall be covered and sealed to provide and insure the integrity of the settings and prevent accidental contact.

- F. Each Vital Processor Unit shall be equipped with Vital Lamp Driver Printed Circuit Boards (VLD PCBs) as specified herein.
 - 1. VLD PCBs shall be furnished and installed in sufficient number to accommodate all vital signal lamps within the Vital Processors Unit's scope of control.
 - 2. The VLD PCBs shall output energy directly to the signal lamps as described herein through the specified cables and internal signal instrument house wiring.
 - 3. The allowable wattage for VLD PCB outputs shall be adequate to handle the designed maximum lamp load for the Contract, as approved by the Engineer.

2.07 FACTORY TESTING

- A. General: Testing shall be in accordance with Section 01 45 24 - Testing Program Requirements.
- B. The VMIS and all subsystems shall be tested in accordance with the approved Factory Test Procedure and with the applicable BART testing requirements.

- C. The VMIS shall be in compliance with and have means of accessibility to permit all testing as required by the current edition of the "Rules and Regulations Governing Railroad Signal and Train Control Systems" as issued by the Federal Railroad Administration. If the Contractor's system requires any external equipment to permit making such tests then such equipment shall be furnished as part of the system.

PART 3 - EXECUTION

3.01 INSTALLATION

- A. The card files shall be mounted in standard 19-inch instrument racks.
- B. All cables or wiring leaving the instrument racks shall be routed through rubber boots at the top of the racks and shall be neatly routed and securely fastened with tie straps.
- C. The mounting of card files and associated equipment shall provide for easy access to all test points, indicators, and adjustments.
- D. Mounting height of microprocessor equipment within a signal instrument house or room shall be restricted to an area between 2.5 feet and 5.5 feet above the finished floor.

3.02 IDENTIFICATION

- A. Card files shall be supplied with a printed label that identifies the input and output ports on the PCB by the name assigned to the port in the application firmware.
- B. Ports shall be identified by the slot number of the PCB and the port number on the PCB.
- C. A method, as approved by the Engineer, shall be used to mount a typed, or printed, name tag on a front plate of each rack or cabinet.

3.03 FIELD TESTING

- A. General: Testing shall be in accordance with Section 01 45 24 - Testing Program Requirements.
- B. The VMIS and all subsystems shall be tested in accordance with the approved Installation Test Procedure and the BART testing requirements.
- C. The latest type test unit for testing vital microprocessor interlocking equipment, as recommended by the manufacturer, shall be furnished to the Engineer, to assist diagnosing modules during a failure mode. This unit shall be designated the remote diagnostics terminal. The remote diagnostics terminal shall be configured for local and remote diagnostics. The remote diagnostics terminal hardware shall be as defined for, but separate hardware from, the lap-top PC specified for the ERS AHCW Analyzer interface computer. All controls required for normal diagnostic inquiries shall be in English dialogue.

END OF SECTION 34 42 19